WHAT IS CLAIMED IS:

1. A device comprising:
a package module having a footprint size based on a standard package;
an unpackaged semiconductor die directly attached to the package module; and
a packaged semiconductor attached to the multi-die module.

2. The device as in Claim 1, wherein the packaged semiconductor is packaged in a ball grid array package.

3. The device as in Claim 1, wherein the unpackaged semiconductor die is a graphics-processor.

4. The device as in Claim 1, wherein the packaged semiconductor is a memory.

5. The device as in Claim 1, wherein a plurality of packaged semiconductors are attached to the multi-die module.

6. The device as in Claim 1, wherein directly attached includes wire bonded.

7. The device as in Claim 1, wherein directly attached includes flip-chip attachment.

8. The device as in Claim 1, wherein attached includes surface-mount technology reflow.

9. The device as in Claim 1, wherein the unpackaged semiconductor die is encapsulated.

10. The device as in Claim 1, wherein the unpackaged semiconductor die is underfilled.

11. The device as in Claim 1, wherein the footprint size of the package module is one of 35mm X 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X 42mm, or 42.5mm X 42.5mm.

12. The device as in Claim 1, further including a heat sink.

13. The device as in Claim 12, wherein a top surface of the unpackaged semiconductor die and a top surface of the packaged semiconductor are of substantially equal distance from a surface of the package module.

14. The device as in Claim 12, further including a shim positioned over the unpackaged semiconductor die such that a top of the shim and a top surface of the packaged semiconductor are of substantially equal distance from a surface of the multi-die module.

15. A device comprising:
a package module sized to be interchangeable with standard package sizes;
a graphics-processing die directly attached to the package module; and
a packaged memory attached to the package module.

16. The device as in Claim 15, wherein the packaged memory is packaged in a ball grid array package.

17. The device as in Claim 15, wherein a plurality of packaged memory are attached to the multi-die module.

18. The device as in Claim 15, wherein directly attached includes wire bonded.

19. The device as in Claim 15, wherein directly attached includes flip-chip attachment.

20. The device as in Claim 15, wherein attached includes surface-mount technology reflow.

21. The device as in Claim 15, wherein the graphics-processing die is encapsulated.

22. The device as in Claim 15, wherein the graphics-processing die is underfilled.

23. The device as in Claim 15, wherein the standard package sizes include one of 35mm X 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X 42mm, or 42.5mm X 42.5mm.

24. The device as in Claim 15, further including a heat sink.

25. The device as in Claim 24, wherein a top surface of the graphics-processor die and a top surface of the packaged memory are of substantially equal distance from a surface of the package module.

26. The device as in Claim 24, further including a shim positioned on top of the graphics-processor die such that a top of the shim and a top surface of the packaged memory are of substantially equal distance from a surface of the package module.

27. A method comprising the steps of:
directly attaching a first semiconductor die to a package substrate;
forming electrical connections between the first semiconductor die and the package substrate;
securing the electrical connections;
placing a second semiconductor die in a die package;
attaching the die package to the package substrate; and
forming electrical connections between the die package and the package substrate.

28. The method as in Claim 27, wherein the step of placing the second semiconductor die in a die package includes placing the semiconductor die in a ball grid array package.

29. The method as in Claim 27, wherein the steps of directly attaching and forming electrical connections are performed using a flip-chip process.

30. The method as in Claim 27, wherein the steps of attaching and forming electrical connections are performed using surface mount technology reflow.

31. The method as in Claim 27, wherein the step of directly attaching includes the use of adhesives.

32. The method as in Claim 27, wherein the steps of forming electrical connections include wire-bonding.

33. The method as in Claim 27, wherein securing the electrical connections includes encapsulating the first semiconductor die.

34. The method as in Claim 27, wherein securing the electrical connections includes underfilling the first semiconductor die.

35. The method as in Claim 27, further including the step of attaching solder balls to an underside of the package substrate.

36. The method as in Claim 27, wherein the package substrate has a footprint of one of 35mm X 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X 42mm, or 42.5mm X 42.5mm.

37. The method as in Claim 27, further including the step of attaching a heat sink to the package substrate.

38. The method as in Claim 37, further including the step of positioning a shim on top of the first semiconductor die such that a top of the shim and a top surface of the die package are of substantially equal distance from a surface of the package substrate.

39. The method as in Claim 27, further including the step of testing the first semiconductor die prior to the step of attaching the die package to the package substrate.

40. The method as in Claim 27, further including the step of testing the second semiconductor die after the step of placing the second semiconductor die in a die package and prior to the step of attaching the die package.